Energy Research and Development Division
FINAL PROJECT REPORT

ADVANCED EPI TOOLS FOR GALLIUM NITRIDE LIGHT EMITTING DIODE DEVICES

Prepared for: California Energy Commission
Prepared by: Applied Materials, Inc.

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PREFACE

The California Energy Commission Energy Research and Development Division supports public interest energy research and development that will help improve the quality of life in California by bringing environmentally safe, affordable, and reliable energy services and products to the marketplace.

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- Renewable Energy Technologies
- Transportation

Advanced EPI Tools for Gallium Nitride Light Emitting Diode Devices is the final report for the grant, PIR-10-055, conducted by Applied Materials Incorporated. The information from this project contributes to Energy Research and Development Division's Buildings End-Use Energy Efficiency Program.

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ABSTRACT

For light emitting diodes (LEDs) to realize its potential in lowering energy consumption and becoming the standard for general lighting needs, it is generally agreed that costs to the consumer must come down significantly. When Applied Materials Incorporated (Applied Materials) conducted a comprehensive review of the value chain of the LED bulb, it was clear that Gallium Nitride (GaN) deposition costs were a significant driver in the final cost of the bulb. The costs not only include tool cost, but the yield and performance of the chips out of the tool.

The overall goal of this project was to develop, build, and demonstrate an improved manufacturing system for GaN power devices such as LEDs. Applied Materials designed, demonstrated and validated the system performance of the full LED Epitaxy (epi) process.

The project accomplished its goals and resulted in successfully building a world-class, epi system that produces high quality LEDs at a lower cost which is now commercially available.

Keywords: LEDs, Light Emitting Diodes, Applied Materials, solid state lighting, GaN LED manufacturing

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EXECUTIVE SUMMARY

Introduction

The California Energy Commission (Energy Commission) provided cost share funding to supplement Applied Materials, Incorporated's (Applied Materials) American Recovery and Reinvestment Act of 2009 (ARRA) award. The purpose of the project was to conduct research and development of a new, more cost effective process for manufacturing Gallium Nitride (GaN) power devices such as Light Emitting Diodes (LEDs). The Energy Commission's cost share assisted in the design and development of a new method to produce high quality light emitting diodes at a lower cost.

The project resulted in the demonstration of a prototype tool that can deposit high-quality GaN materials on at least two different substrate materials. This new advanced system will enable LED manufacturers to fabricate higher-quality LED devices at a lower cost, and help address a major obstacle to widespread adoption of high quality and more energy efficient LEDs. This project accomplished the goals of designing, validating and developing improved GaN manufacturing process equipment that is now commercially available.

Wide spread adoption of LEDs could significantly reduce energy use associated with lighting. The LED technology is an efficient light source over other technologies such as incandescent. Incandescent lighting produces up to 18 lumens of light output for every watt of energy it consumes while LEDs produce up to 100 lumens for every watt.

Energy Commission funding was critical to retain jobs during a down economy at Applied Materials' Research and Development facility in Santa Clara, California. By 2015, Applied Materials estimates that 350 employees will be assigned to the product that resulted from this project. About one-half of the employees will be in Santa Clara, California. These employees will work in engineering, manufacturing, service and maintenance, technology, marketing, administration, and critical support functions such as finance, human resources, and legal counsel.

Appendix A contains a copy of the final report, Advanced Epi Tools for Gallium Nitride Light Emitting Diode Devices, prepared by Applied Materials for the U. S. Department of Energy under grant DE – EE0003331.

APPENDIX A:
Applied Materials Report to U.S. Department of Energy

Submitted to the U. S. Department of Energy, Agreement DE-EE0003331, December 7, 2012

Solid State Lighting Program
FINAL REPORT

December 7, 2012

Advanced Epi Tools for Gallium Nitride Light Emitting Diode Devices

Work Performed Under Agreement:
DE- EE0003331

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Disclaimer:

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Executive Summary

Over the course of this program, Applied Materials, Inc., with generous support from the United States Department of Energy, developed a world-class three chamber III-Nitride epi cluster tool for low-cost, high volume GaN growth for the solid state lighting industry. One of the major achievements of the program was to design, build, and demonstrate the world's largest wafer capacity HVPE chamber suitable for repeatable high volume III-Nitride template and device manufacturing.

Applied Materials' experience in developing deposition chambers for the silicon chip industry over many decades resulted in many orders of magnitude reductions in the price of transistors. That experience and understanding was used in developing this GaN epi deposition tool. The multi-chamber approach, which continues to be unique in the ability of the each chamber to deposit a section of the full device structure, unlike other cluster tools, allows for extreme flexibility in the manufacturing process. This robust architecture is suitable for not just the LED industry, but GaN power devices as well, both horizontal and vertical designs.

The new HVPE technology developed allows GaN to be grown at a rate unheard of with MOCVD, up to 20x the typical MOCVD rates of 3µm per hour, with bulk crystal quality better than the highest-quality commercial GaN films grown by MOCVD at a much cheaper overall cost. This is a unique development as the HVPE process has been known for decades, but never successfully commercially developed for high volume manufacturing. This research shows the potential of the first commercial-grade HVPE chamber, an elusive goal for III-V researchers and those wanting to capitalize on the promise of HVPE.

Additionally, in the course of this program, Applied Materials built two MOCVD chambers, in addition to the HVPE chamber, and a robot that moves wafers between them. The MOCVD chambers demonstrated industry-leading wavelength yield for GaN based LED wafers and industry-leading uptime enabled in part by a novel in-situ cleaning process developed in this program.

The Department of Energy was a great supporter of this leading-edge technology that can benefit U.S. industry and keep GaN manufacturing competitive in the United States. We gratefully acknowledge their role in advancing the state-of-the-art.

Program Goals and Accomplishments

Overview

For solid state lighting to realize its potential in lowering energy consumption for the nation and becoming the standard for general lighting needs, it is generally agreed that costs to the consumer must come down significantly. When Applied Materials did a comprehensive review of the value chain of the LED bulb, it was clear that GaN deposition costs were a significant driver in the final cost of the bulb. The costs not only include tool cost, but the yield and performance of the chips out of the tool.

The overall goal of this program was to develop, build, and demonstrate a low-cost manufacturing system for GaN LED manufacturing. Not only did we design a system, but validate the system by developing a full LED epi process. We set this high bar of actually demonstrating world-class device performance because of the reputation Applied Materials has built over many decades as the leader in high volume nano-scale manufacturing. Without developing a process, and given the fact that Applied Materials was new to this market, we could not validate the world-class nature of our system.

We are happy to report that we accomplished the goals we set out to accomplish in this successful program, building a world-class, low-cost epi system for GaN LEDs that has shipped to customers world-wide. We describe our achievements in more detail below.

Our approach was fundamentally different than the standard approach in two ways. First, Applied Materials would use the cluster approach that it has successfully implemented in the silicon industry, driving down manufacturing costs by orders of magnitude and enabling the information age. Secondly, we would develop the world's first manufacturing-grade HVPE chamber to increase the rate of GaN deposition by over an order of magnitude, further driving down epi manufacturing costs for the LED industry.

Program Goals

There were five milestones proposed at the start of this program in 2010. We are happy to report that we exceeded expectations for all of them. This program was unique in that Applied Materials not only designed new epi chamber architectures, but developed GaN process and GaN devices to show the viability of the tool design. This feedback loop was a key to the success of the program and sometimes not recognized as a necessary requirement. The key achievements for each milestone are highlighted below.

Milestone 1: Multi-wafer HVPE Epi Chamber

Goal

Increase manufacturing throughput by developing and assembling a multi-wafer hydride vapor phase epitaxy (HVPE) system that can deposit high-quality GaN with a growth rate twice as fast as an MOCVD system.

Accomplishments

Table 1 summarizes the achievements in designing and building the world's largest wafer capacity HVPE chamber that was demonstrated to grow thick GaN layers of exceptional quality with operating costs significantly below MOCVD.

Table 1: Summary of HVPE Accomplishments

Feature	Typical MOCVD	Applied HVPE
Growth Rate	2-3 μm/hr	10 - 100 μm/hr
Crystal Quality (on PSS)	~ 250" (102)	~ 150" (102)
Thickness per run	4-6 μm	4-30 μm
Precursor Cost	Trimethylgallium (TMG)	Ga, >5x less than TMG

Key advancements in the proprietary Applied Materials HVPE technology include:

1. Fast GaN deposition rates for high throughput and productivity
2. Unique in-situ HVPE buffer techniques for GaN deposition on planar sapphire and PSS
3. Excellent u-GaN/n-GaN crystalline quality on planar sapphire wafers with XRD FWHM for (002) of 90-130" and (102) of 200-250"
4. Excellent u-GaN/n-GaN crystalline quality on patterned sapphire substrate (PSS) with XRD FWHM for (002) of 170" and (102) of 150"
5. Smooth GaN morphology
6. Improvement of light extraction
7. Lower defect densities for IQE, leakage current improvement
8. Process flexibility for wide range of u- and n-GaN thicknesses, and high Si n-doping levels
9. Production HVPE tool with high capacity : 31 x 2", 8 x 4", 4 x 6", 1 x 8"

GaN Thickness Uniformity.

The final HVPE chamber design and process gas delivery systems was chosen and optimized after investigating many different options. Figure 1 shows the GaN thickness uniformity that was achieved with our final design. The carrier in the chamber accommodated 31 two inch sapphire wafers and we report a radial 1-σ uniformity of 1.4%. The design of the chamber led to radial variations from the center of the chamber outward, which were optimized. The thickness uniformity maps for GaN layers grown on four 2 inch planar sapphire substrates located in four pockets across the carrier are shown in Figure 1. Within wafer thickness uniformity is within 1.2%, 1-σ.

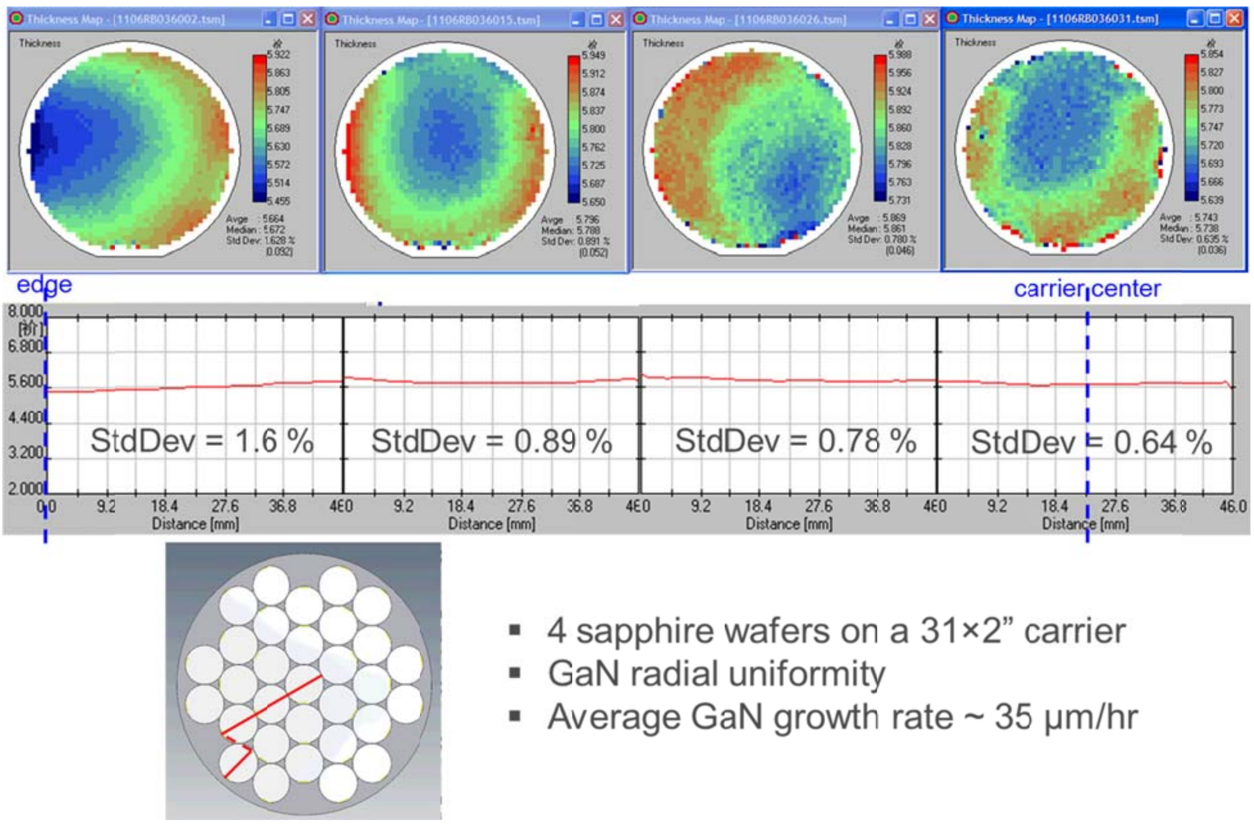


Figure 1: 4-wafer radial thickness uniformity data based on a HVPE GaN run on a 31×2-in carrier. The within-platter (WiP) weighted uniformity 1-σ here is 1.4%; while average within-wafer (WiW) 1-σ is 1.2%.

GaN Crystalline Quality

Optimization of the HVPE in-situ buffer techniques gave us the opportunity to grow GaN material with excellent crystalline quality on planar sapphire. Fig. 2 shows excellent run-to-run repeatability of GaN crystal quality (XRD RC FWHM) for u-/n-GaN structure grown with proprietary in-situ HVPE buffer on planar 2 inch sapphire substrates. This is evidence of the production worthiness of the HVPE chamber. The total thickness of the u-/n-GaN structure is 7 μm (the thickness of n-GaN is about 3.5 μm with doping carrier concentration of 5E18 atom/cm^3).

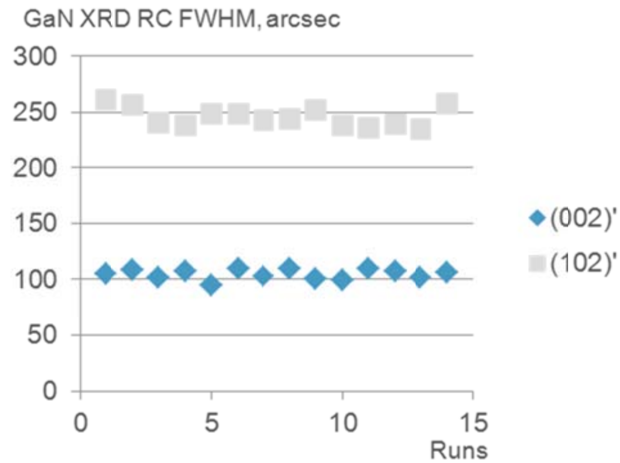


Figure 2: HVPE GaN XRD RC FWHM for 7 μm thick u-/n-GaN structure grown with proprietary in-situ buffer on planar 2 inch sapphire substrates in 14 repeatable deposition runs. The in-situ Cl_2 based chamber cleaning recipe was applied after each deposition run.

Milestone 2: HVPE and MOCVD Device Integration

Goal

Decrease cycle time and improve binning yield by demonstrating a three-chamber MOCVD / HVPE+MOCVD system and a manufacturing process that can produce LEDs with (a) internal quantum efficiency of 75% and (b) PL wavelength uniformity variation of < 1.5nm, 1σ within each wafer and wafer-to-wafer.

Accomplishments

Device Performance.

Validation of our epitaxial tool architecture required developing world-class LED's in addition to the advanced design of the chambers. This was a challenge that other GaN epi chamber manufacturers would not have required. However, because we were not an established playing in the LED industry, our customers required that we demonstrate world-class device performance in addition to high volume, production-worthy chambers.

Figures 3 and 4 show the quality of LED's able to be achieved in the Applied Materials multi-chamber tool with performance of 88% IQE and 57% EQE, among the best in the industry, clearly showing the capability using the epi equipment developed under this program for High Volume Manufacturing.

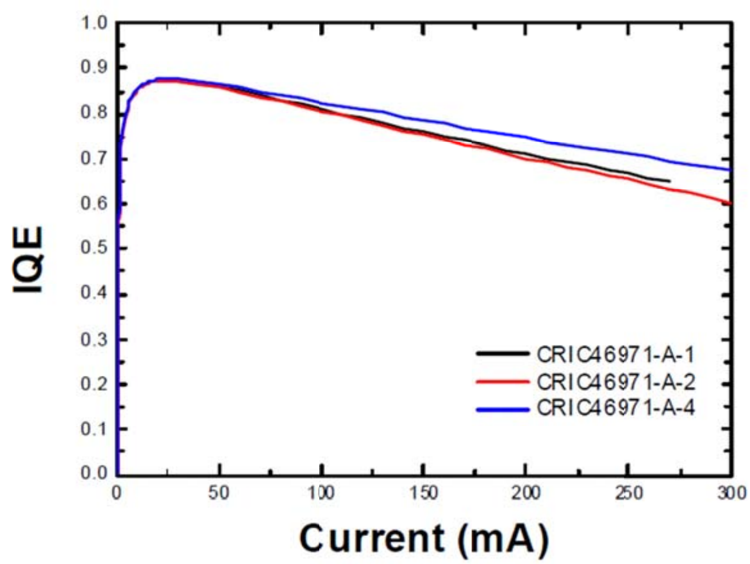


Figure 3: 88% IQE Demonstrated on LEDs from the Applied Materials Cluster Tool

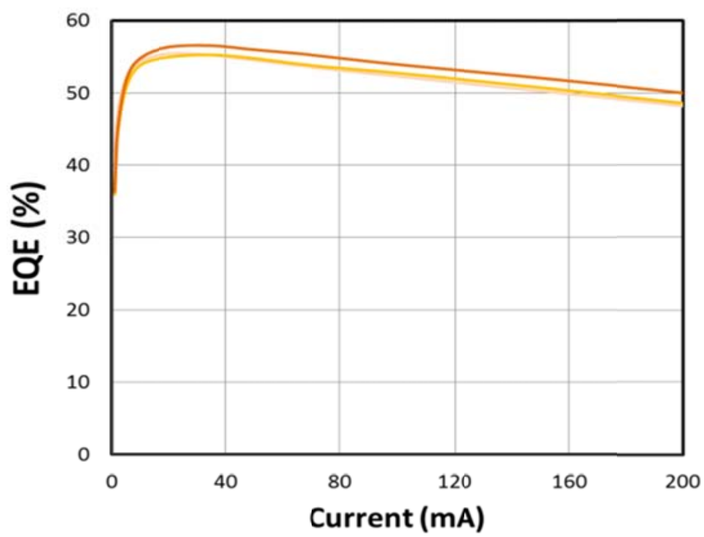


Figure 4: 57% EQE Demonstrated on LEDs from the Applied Materials Cluster Tool

Hands-Off 120 Consecutive Runs

High-volume production requires tools that can perform the required task(s) with minimum assistance from an operator, technician or process engineer. A key measurement of the "hand-off" operation of the LED epi system being developed under this program was accomplished in MOCVD, starting with 10 runs and ending with the hands-off mode at 120 runs, a significant achievement.

Hands off means that the only task for the operator was to place the wafer cassette holding the "to be processed" wafers on the automated wafer loading mechanism and then remove them after they were processed. There were no recipe adjustments or tweaks allowed and the chamber remained closed during the entire proceedings. As can be seen in Figure 5, we first successfully processed 60 runs in hands off mode, performed an 8 hour periodic maintenance and then proceeded to run 120 additional hands-off runs. This was accomplished by design improvements of the chambers in addition to the *in-situ* clean process, Milestone 4. The combination of these two actions resulted in the performance shown.

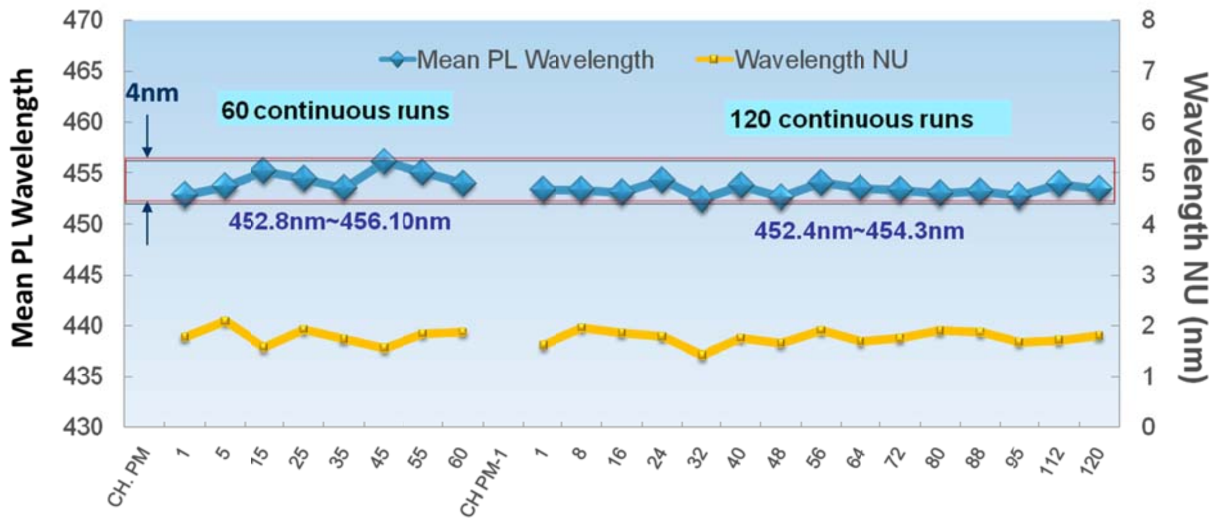


Figure 5: A key achievement of the program: 60 and 120 continuous "hands-off" runs with exceptional wavelength uniformity and no opening of the chamber.

The hands-off 12- consecutive runs is a major improvement over the operation of conventional systems and the frequent intervention for manual cleaning, parts replacement, chamber seasoning, and epi recipe adjustments. This capability was a significant factor in reaching various Milestones throughout the program.

High Quality MQW

Another major result of the multi-chamber progressive process is the precision brought to the gas flow and temperature control during MQW growth. Figure 6 shows the consistency in the MQW layer which is controlled by both gas flows and ultra-precise thermal control. The configuration of the system with fast response radiant heating is creating strong results for MQW consistency.

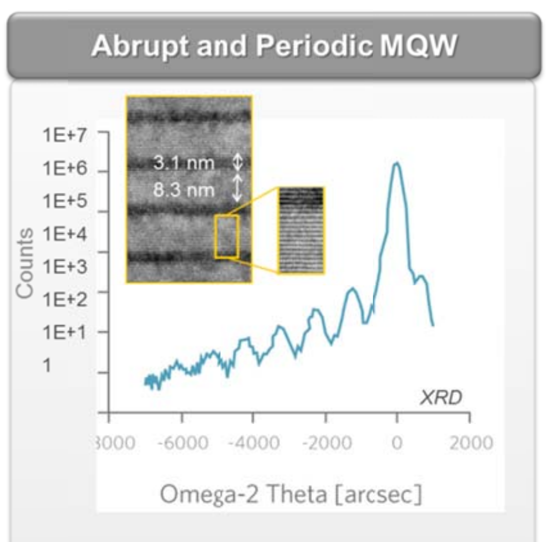


Figure 6: MQW SEM cross section and periodicity

PL Results

Figure 7 shows the wavelength uniformity from a series of runs with a number of wafers to examine cumulative PL performance. The results showed 86.9% of all points were located in a 5 nm bin around the targeted 450nm value, clearly demonstrating exceptional binning capabilities for LED manufacturers. Figure 8 shows the wavelength uniformity within a single carrier and a min-max variation of 12.5nm.

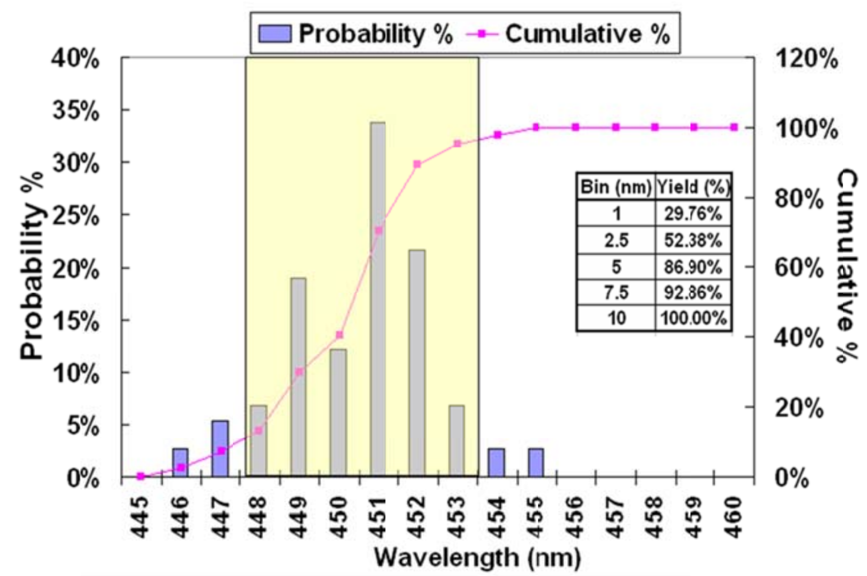


Figure 7: Distribution of PL for Wavelength

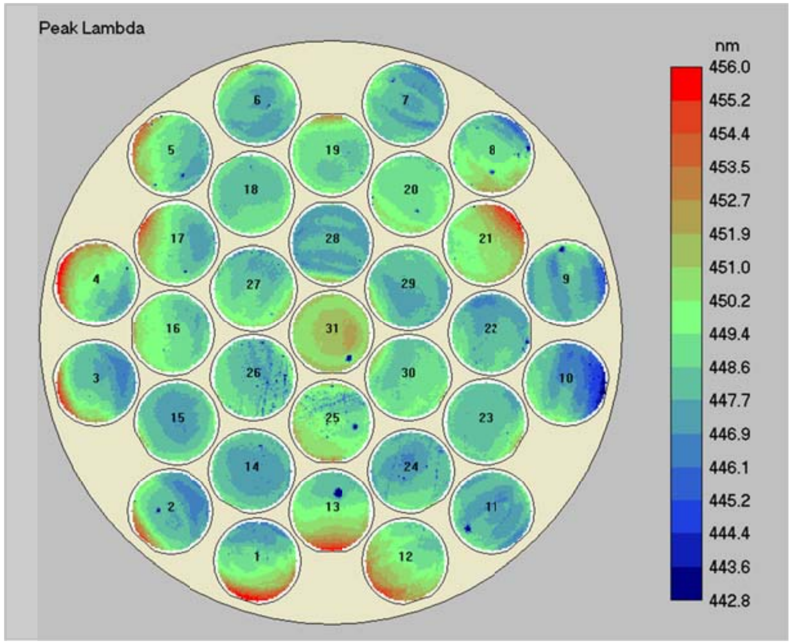


Figure 8: Full carrier mapping of wavelength showing exceptional min-max binning of 12.5nm

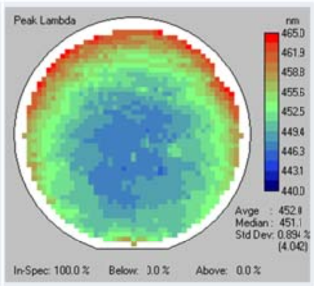
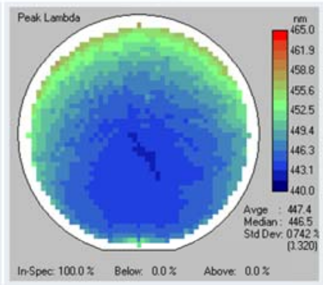
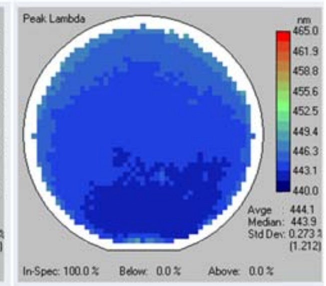
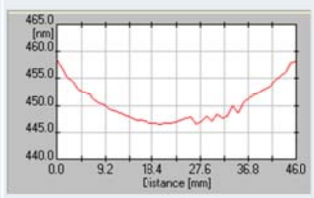
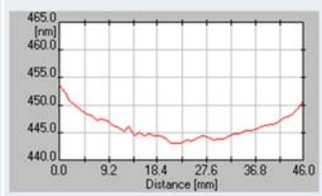
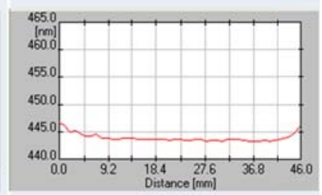
Bow

Typically, lattice mismatch and thermally induced stress during MOCVD LED growth results in wafer bending, defect formation, or even film cracking. An important impact of wafer bending during growth is the change of thermal contact between the wafer and the substrate holder. This is especially important for indium-containing compounds, since indium incorporation during MOCVD growth is known to be very temperature sensitive. Therefore, wafer bow control at InGaN MQW growth conditions is required for good in wafer wavelength uniformity.

In order to verify the impact of wafer curvature during our HVPE+MOCVD integration growth on wavelength uniformity, we used HVPE u-GaN/n-GaN templates with different room temperature bow for subsequent MOCVD InGaN multiple quantum well structure growth.

The stress during HVPE growth (and as a result, the bow of u-GaN/n-GaN templates) was managed by changing of HVPE process parameters during in-situ buffer steps. In some runs the bow was also managed by changing of u-GaN/n-GaN thickness and a range of room temperature convex bow height was used- 8 to 60 μm. The templates were characterized by ex situ optical bow measurements at room temperature and transferred to the MOCVD chamber for multiple quantum well test structure growth. Table 2 shows the PL mapping and wavelength line profile across the 2" wafer for InGaN multiple quantum well structures grown on HVPE u-GaN/n-GaN templates.

Table 2: PL mapping and wavelength profile across the 2" sapphire substrate for InGaN multiple quantum well structures grown on HVPE u-GaN/n-GaN templates

MOCVD run ID	6RD018-21	6RD018-23	6RD018-25
HVPE Template ID	3RB036-13	3RB038-13	6RB004-17
WL (nm)	457	453	450.3
WL Uniformity (nm)	3.57	2.77	0.95
Bow Height (um)	9	26	51
WLP Contour Map			
Line Profile of WLP			

Three HVPE u-GaN/n-GaN templates had different convex bow height: 9, 26 and 51 μm. After subsequent InGaN multiple quantum well structure deposition on the top of HVPE templates, all templates revealed different behavior in terms of wavelength uniformity. While the low convex bow (9 μm) template exhibits a considerable concave wavelength profile and high wavelength STD (3.57 nm) the wavelength profile for high convex bow (51 μm) template is nearly flat. As a result, the wavelength STD is low (0.95 nm) for this template.

The considerable concave wavelength profile (or red shift of the PL wavelength in the wafer center) can be correlated to the convex wafer shape at InGaN MQW growth conditions. Assuming that the wafer center is cooler than the wafer edges in the case of convex bowing (at InGaN MQW growth conditions) a higher indium concentration can be expected. The flat wavelength profile can be correlated to a flat wafer shape (and uniform temperature distribution across the wafer) at InGaN MQW growth conditions.

So, with stress control during HVPE growth, we were able to optimize the temperature distribution across the wafer during MOCVD GaInN MQW growth and achieve high wavelength uniformity.

To verify the w-to-w and run-to-run wavelength uniformity asequence of three HVPE and three MOCVD runs was conducted in AMAT cluster tool. Six 2 inch sapphire substrates for each run were placed on 31x2" carrier and transferred to HVPE chamber. After 6 μm thick u-GaN/n-GaN deposition in HVPE chamber at optimized (for stress control) conditions, the carrier with six HVPE templates (located across the carrier) was transferred to MOCVD chamber. The test LED structures were deposited in MOCVD chamber and characterized by ex-situ PL. The PL wavelength uniformity data for three MOCVD runs are presented at Table 3.

Table 3: The PL wavelength uniformity data from LED structures grown on HVPE u-GaN/n-GaN templates in three MOCVD runs

		Run ID	6MA079	Run ID	6MA080	Run ID	6MA081
	Wafer ID	Wavelength (nm)	STD (nm)	Wavelength (nm)	STD (nm)	Wavelength (nm)	STD (nm)
	2	448	1.11	446	1.23	447.9	1.58
	14	445.6	1.05	444.7	1.22	445.8	1.42
	25	445.5	1.32	444.1	1.6	444.1	1.9
	27	444.8	1.16	444.8	1.68	444	1.93
	17	446.4	1.13	445.9	1.08	444.6	1.23
	5	447.6	1.85	448.6	1.8	448.3	1.15
Average		446.32	1.27	445.68	1.44	445.78	1.54
W-to-W uniformity (nm)			1.26		1.61		1.91

The average data for PL wavelength uniformity are presented at Table 4. The within wafer uniformity and run-to-run uniformity have achieved the target. The wafer-to-wafer uniformity is close to the target and can be improved by additional tuning.

Table 4:Average data for PL wavelength uniformity of integrated HVPE/MOCVD runs

Uniformity	Within Wafer	Wafer-to-Wafer	Run-to-Run
Result (nm)	1.41	1.59	0.34
Target (nm)	1.5	1.0	1.4

A quick EL apparatus is used to measure the EL wavelength at 5 points across the wafer and the wavelength STD is calculated. Table 4 is an example of EL measurement of a wafer from the integrated HVPE/MOCVD run. It shows the EL STD of HVPE and MOCVD can achieve 1.15 nm which exceeds the target of 1.5 nm.

Table 5: EL and PL wavelength measurement

PL WLD (nm)	PL WLD u% (nm)	EL WLD @10mW (nm)	EL WLD STD 5pts (nm)
449.2	0.856	448.8	1.15

In summary, the impact of wafer curvature during growth of a LED test structure on wavelength uniformity across the wafer was demonstrated. With stress control during HVPE growth, we were able to optimize the temperature distribution across the wafer during MOCVD InGaN MQW growth and reach specification target for PL wavelength uniformity.

Milestone 3: Second Substrate Demonstration

Goal

Assure the industrial relevance of the three-chamber MOCVD / HVPE system developed for Milestone 2 by developing processes that allow it to deposit high-quality LED structures on the most promising alternate substrate material.

Accomplishments

Over the course of this program, we investigated a variety of alternate substrates in addition to standard two-inch planar sapphire substrates.

Growth of HPVE GaN on PSS

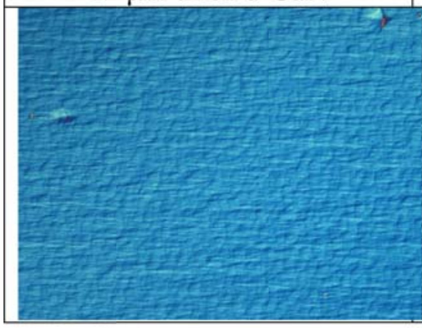
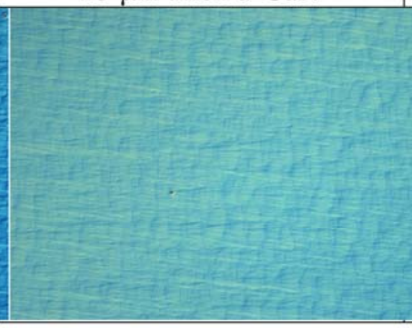
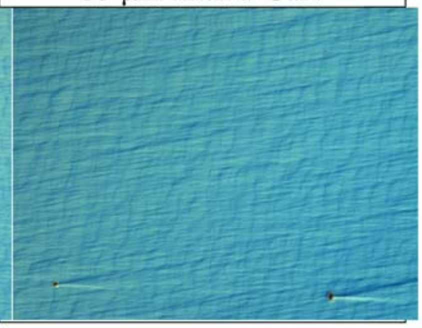
We started the investigation of u-GaN deposition on 2" PSS in the HVPE chamber to validate the feasibility for LED customers. Three different in situ HVPE buffer concepts were investigated and Table 6 shows XRD rocking curves for (002) and (102).

Table 6:XRD data of u-GaN grown on PSS using HVPE

Buffer type	Runs ID	GaN Thickness (um)	Rocking Curves (XRD arcsec)	
			(002)	(102)
A	RB33	6	196.8	185.6
B	RB34	9.7	306.9	199.9
C	RB47	7.6	221.3	138.7

The results show how the crystal quality can be engineered to extremely low values, among the best in the industry and the deposition rate for PSS was also demonstrated to be 60um/hour. Table 7 shows the excellent flat 2-D morphology of u-GaN layers grown in single deposition runs on PSS with high GaN growth rate (about 60 μm/hour).

Table 7: Optical microscope images of surface of GaN grown on PSS

12 µm thick u-GaN	23 µm thick u-GaN	33 µm thick u-GaN
		

GaN on PSS 4" Sapphire

As we have discussed previously, our Tier-1 customers expressed most interest in 4" sapphire development over other, more exotic substrate options. We were able to fit eight (8) four inch wafers on a platter in a single run. A wavelength uniformity map is shown in Figure 9.

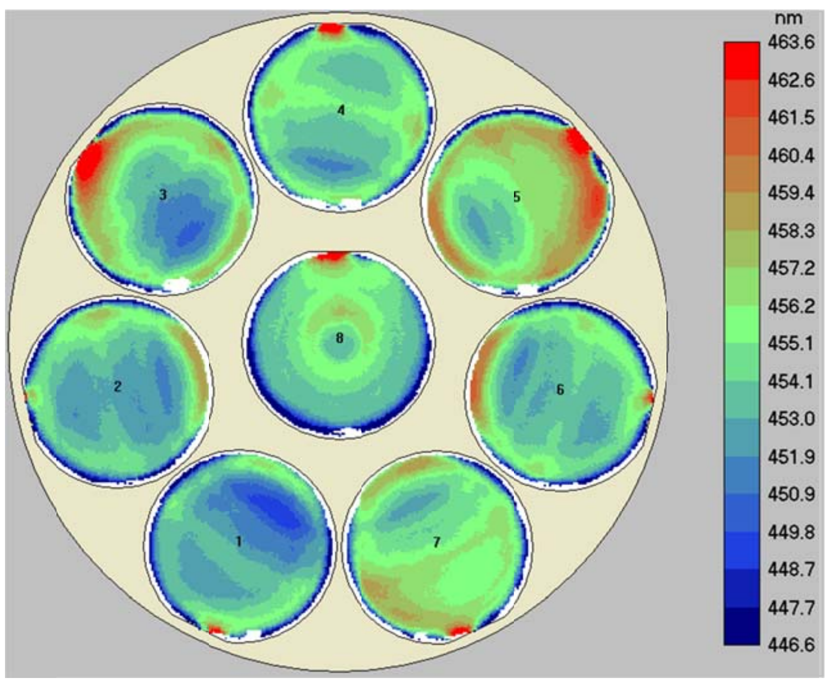


Figure 9: WL uniformity map of 8 x 4" sapphire wafers from a single run

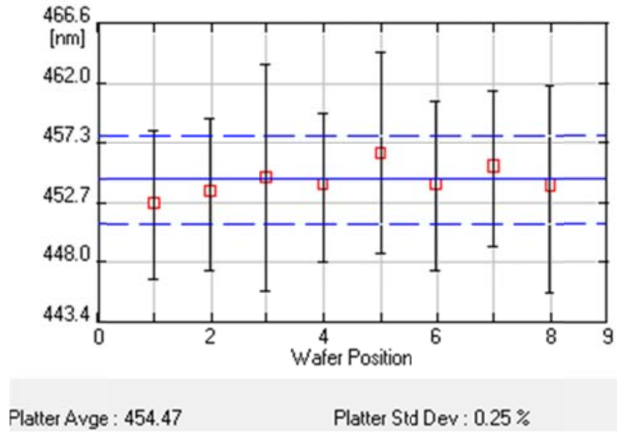


Figure 10: Wavelength Uniformity of each wafer

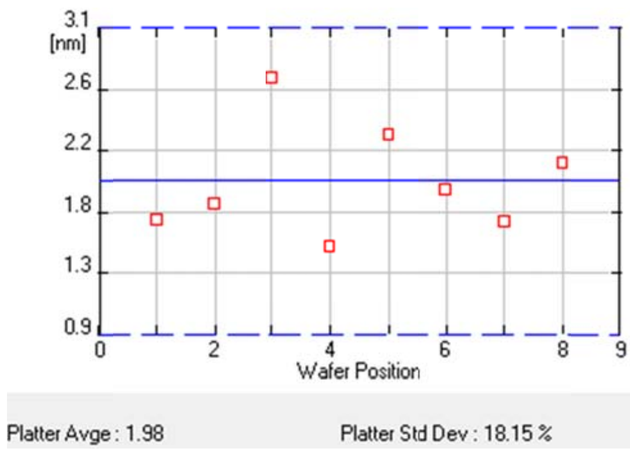


Figure 11: Wavelength Uniformity Standard Deviation

Figures 10 and 11 show that we were able to achieve a 2 nm standard deviation and 4 nm within platter wavelength range with a high brightness recipe. Additional work is still needed to get all the wafers below 2 nm stdev.

GaN on 6" Sapphire

Multiple process kit configurations were tested to achieve the best within wafer (and within platter results) for 6-inch sapphire and to try to match the existing results on 2" wafers. A two zones lamp module was tested for the 4x6" configuration which resulted in lower power consumption when compared to the standard 3-zone lamp module, which would thereby lower operating cost. The best data achieved is shown below in Figures 12 and 13.

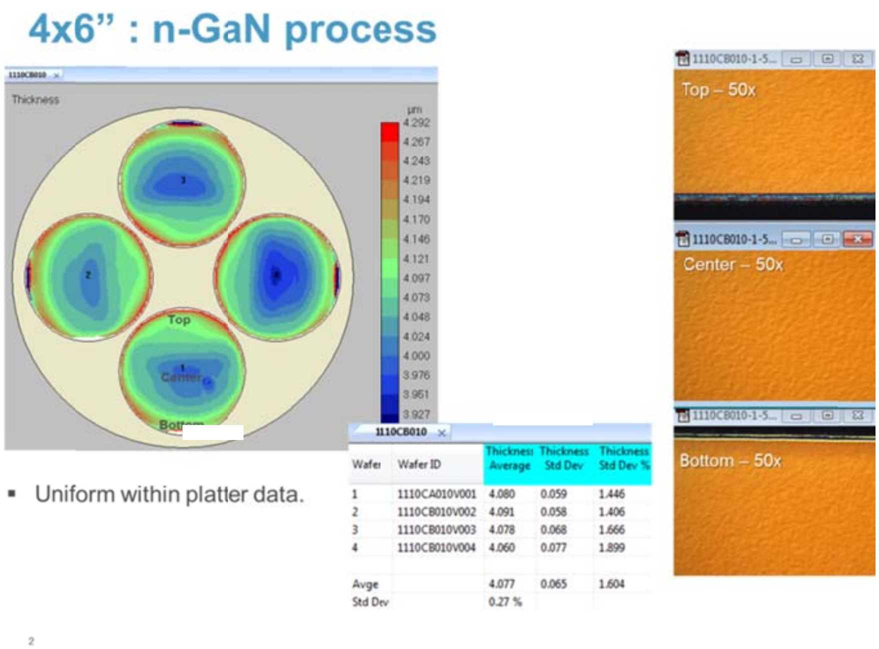


Figure 12: Thickness uniformity of 6" n-GaN wafers

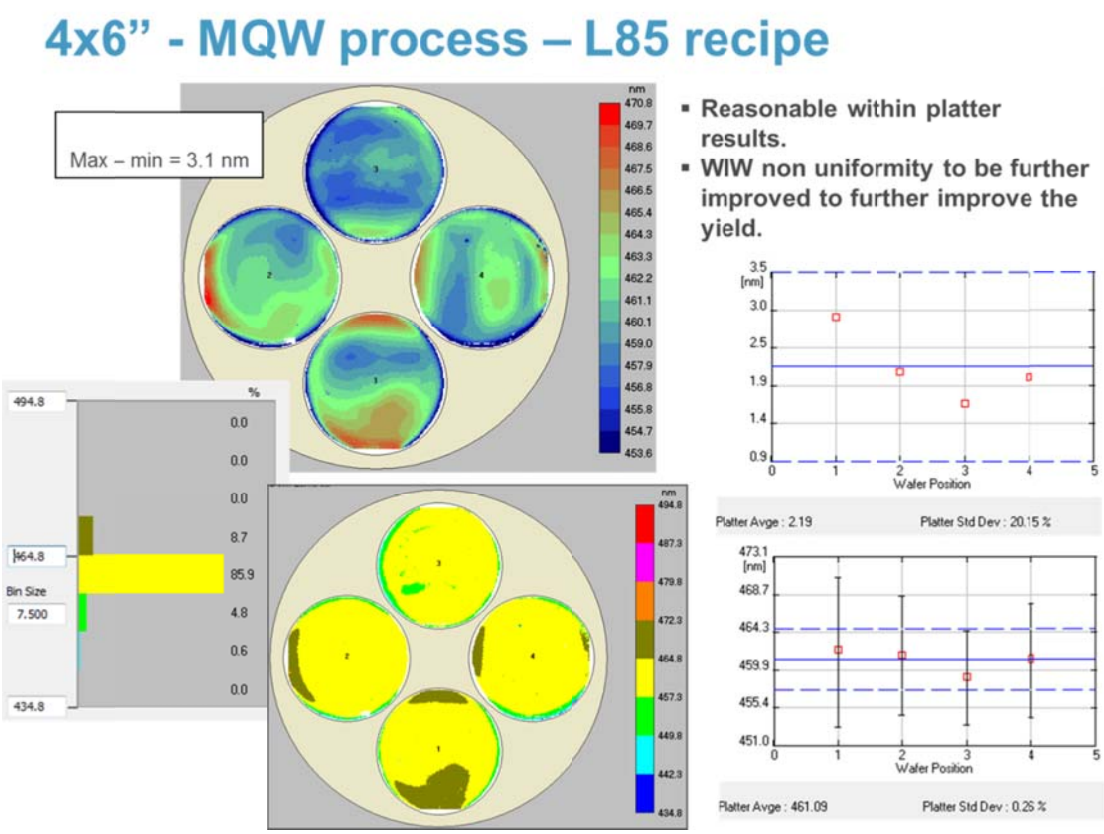


Figure 13: WL uniformity of 6" wafers

GaN on 6" Silicon

We investigated GaN growth on 6-inch Si (111) substrates using a standard MOCVD structure described in the literature:

1. AlN seed layer
2. AlGaN stress control intermediate multi-layer
3. 2.5 μm thick GaN layer

The XRD rocking curve FWHM (in arcsecs) of AlN seed layers and GaN layers grown on Si are shown in Table 8. We also introduced in-situ SiN nanomask layer to improve GaN quality as shown in Table 8-B.

Table 8: GaN on Silicon Results

Sample	Buffer	SiN nanomask?	AlN (002)	GaN (002)	GaN (102)
A	Yes	No	1016	502.2	702
B	Yes	Yes	815.5	381	394.7

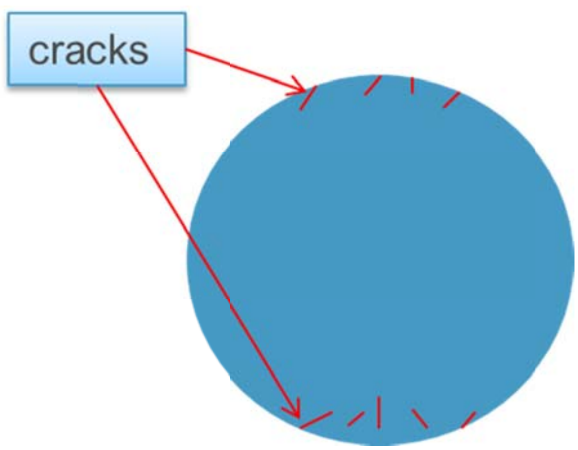


Figure 14: GaN on Silicon edge cracks

Further development is necessary to reduce wafer edge film cracks (Figure 14) as well as improve crystal quality. Of course, GaN on silicon development is a significant challenge on its own, but the Applied Materials cluster tool is well-suited for this substrate because of the multi-chamber flexibility.

Milestone 4: in-situ Clean

Goal

Increase throughput by developing a novel automated *in situ* cleaning process in which the system introduces a gas or gases that react with the GaN deposited on the chamber walls and then exhausts the reactants.

Accomplishments

Applied Materials was able to demonstrate an industry-first *in-situ* GaN cleaning process that allows the LED manufacturer to run the LED epi process with minimal downtime for routine maintenance. The success was demonstrated with the 120 consecutive run results above. The technology utilizes thermally-activated chlorine clean to remove Ga-rich GaN deposits on chamber surfaces as shown in Figure 16.

Two simultaneous processes, chlorination of GaN and sublimation of $GaCl_x$, as shown in Figure 15, and the fast etch rates allow for continuous process runs with minimal changes to the chamber condition, exemplified by the wavelength repeatability run to run. The technology and process requires optimized showerhead temperature, chlorine flux, and chamber pressure, which is unique to each manufacturer's process.

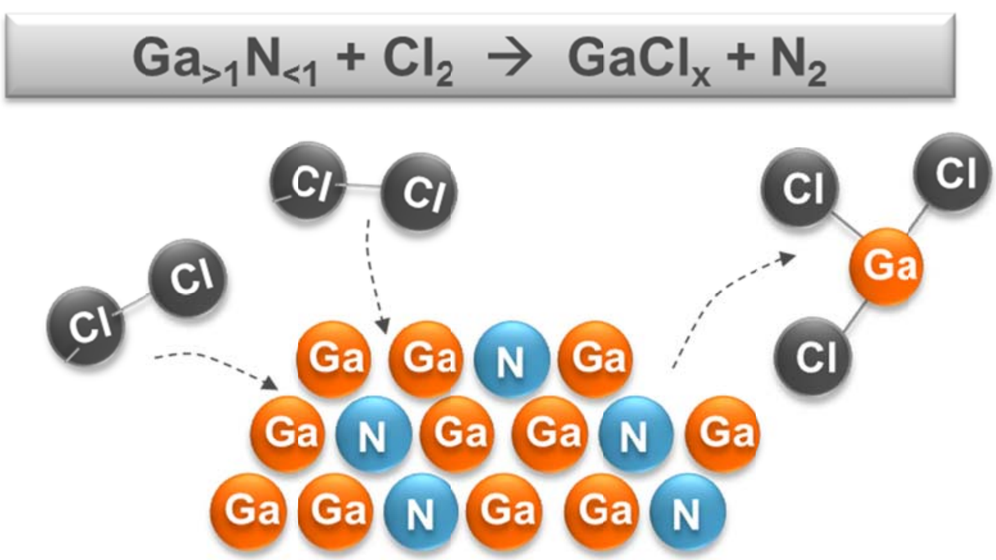


Figure 15: The general process of *in-situ* chlorine clean of the chamber

Figures 16: Before and after *in-situ* clean pictures of the MOCVD showerhead. Note the dark GaN deposits which are cleaned in the "after" picture on the right.

In addition to MOCVD chamber clean, an HVPE in-situ clean was demonstrated with a process design shown in Figure 17.

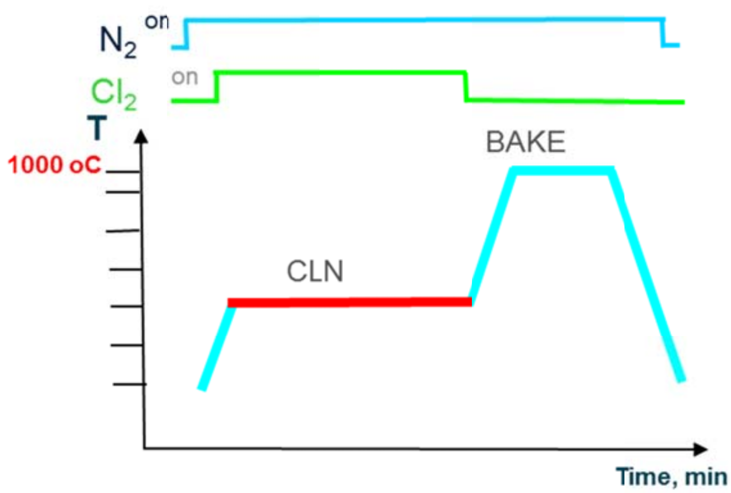


Figure 17: Typical clean cycle in the HVPE chamber

Milestone 5: Optimized Three-Chamber Tool

Goal

Design, build, assemble, and test a full-scale multi chamber epitaxial growth system for LED manufacturing with *in situ* cleaning capability. We will assemble the entire tool, including the gas handling subsystems and the robotic automatic transport. We plan to integrate the control systems of each chamber to create a single control system

Accomplishments

We were proud to demonstrate the three chamber epi tool to the DOE program management team of Dr. Brian Dotson and Dr. Steven Bland during the June, 2012 on-site visit as shown in Figure 18 in our lab in Santa Clara, California. The final HVPE integration validation as described above was performed since the review, requiring a short extension.

Figure 18: The Three Chamber MOCVD + HVPE GaN epi Tool Designed, Built, and Validated under this Program

Cycle Time Reduction

A key goal of the program was to reduce the cycle time of epi manufacturing. By splitting the LED GaN process and dedicating chambers to specific processes, an improvement in cycle time was achieved. For a 3 chamber configuration, one chamber is dedicated to u-GaN/n-GaN deposition by HVPE, a second chamber for MQW (MOCVD), and a third chamber for p-GaN (MOCVD) as shown in Figure 19.

Figure 19: Sequential 3 chamber process ("1 + 1 + 1")

The MQW process time assumes 5 pairs, while the HVPE process time assumed 4 microns are grown in 1 hour. The cycle time per run can be reduced to 3.3 hrs. as shown in Table 9. It should be noted that the u-GaN/n-GaN process includes a 1 hr. chamber clean. Also, the exchange time of 20 seconds for the robot to move carriers through the system has no impact on the cycle time.

Table 9: Schematic for Cycle Time with Dedicated u-GaN/n-GaN , MQW and p-GaN Chambers

Run #	TIME START			Time out	Cycle time (Elapsed Time / # Runs)
	HVPE (2 hrs)	MO MQW (3 hrs)	MO p-GaN (1 hr)		
1	0:00	2:00	5:00	6:00	
2	2:00	5:00	8:00	9:00	4.500
3	4:00	8:00	11:00	12:00	4.000
4	6:00	11:00	14:00	15:00	3.750
5	8:00	14:00	17:00	18:00	3.600
6	10:00	17:00	20:00	21:00	3.500
7	12:00	20:00	23:00	0:00	3.429
8	14:00	23:00	2:00	3:00	3.375
9	16:00	2:00	5:00	6:00	3.333
10	18:00	5:00	8:00	9:00	3.300
etc.	…	…	…	…	…

Further cycle time optimization can be achieved by configuring the multi-chamber tool with one chamber using HVPE to deposit the u-nGaN film, and 2 chambers to deposit via MOCVD *both* MQW and p-GaN layers simultaneously as shown in Figure 20. Table 2 demonstrates that a cycle time of 2.3 hrs. can be achieved, far exceeding the program goal of 3.5 hours by 35%.

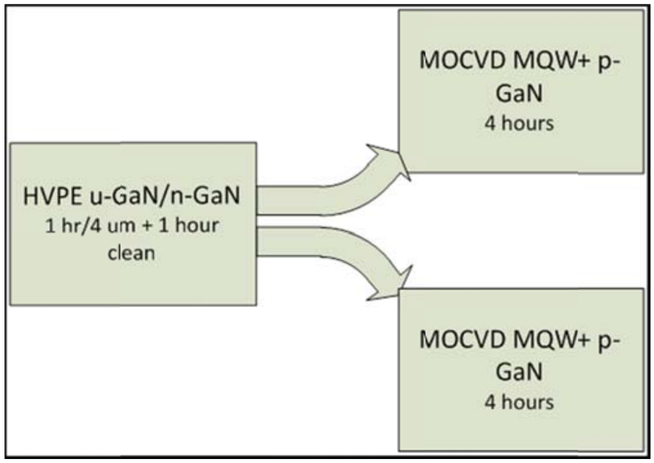


Figure 20: Simultaneous MQW/p-GaN process ("1 x 2")

Table 10: Schematic for Cycle Time with Dedicated u-GaN/n-GaN Chamber and Two MQW-p-GaN Chambers

Run #	TIME START			Time out	Cycle time (Elapsed Time / # Runs)
	HVPE (2 hrs)	MQW + p-GaN (4 hrs)	MQW + p-GaN (4 hrs)		
1	0:00	2:00		6:00	
2	2:00		4:00	8:00	4.000
3	4:00	6:00		10:00	3.333
4	6:00		8:00	12:00	3.000
5	8:00	10:00		14:00	2.800
6	10:00		12:00	16:00	2.667
7	12:00	14:00		18:00	2.571
8	14:00		16:00	20:00	2.500
9	16:00	18:00		22:00	2.444
10	18:00		20:00	0:00	2.400
11	20:00	22:00		2:00	2.364
12	22:00		0:00	4:00	2.333
etc.	…	…	…	…	…

The work we have done previously to optimize chambers #2 and #3 for MQW and p-GaN respectively in the standard sequential process flow is transferrable to the new simultaneous process flow and we are confirming the high quality of resulting LEDs

Project Activity Summary

Original hypotheses

The original Statement of Program Objectives (SOPO) is listed below.

OBJECTIVES

THE RECIPIENT proposes to develop a multi-chamber system such as a two MOCVD chambers, one HVPE chamber, lamp heating, and automated in situ cleaning. The system shall be capable of growing high-quality LEDs on substrate materials currently in commercial use or under consideration. It shall contain a 300-mm or larger platter that holds 28 two-inch wafers. THE RECIPIENT shall build it on the successful Centura (TM) platform, the standard for growing low-cost, high-quality epitaxial wafers in the integrated circuit industry. The proposed system shall decrease operating costs through a combination of decreasing cycle time, increasing throughput, using in-situ cleaning, and decreasing the cost of chemicals. It shall increase the internal quantum efficiency of LEDs by reducing the density of extended defects and point defects. It shall improve binning yields by improving the uniformity of wavelength and output power within the wafer, from wafer to wafer, and from run to run.

TASKS TO BE PERFORMED

Project Management and Planning

THE RECIPIENT shall develop and maintain a Project Management Plan (PMP) throughout the course of the project. The initial PMP shall be submitted to the DOE Project Officer within 60 days of award. The Recipient shall review and update the PMP at the end of each Budget Period and resubmit as a part of the budget period continuation application. The PMP shall also be modified on an ad hoc basis to reflect significant changes or deviations of planning.

Multi-Wafer HVPE Epi Chamber

THE RECIPIENT shall design and assemble a multi-wafer nitride HVPE system for high volume production. The goal shall be to identify a chamber design and compatible process conditions that can deposit high-quality GaN at a growth rate of several microns per hour. THE RECIPIENT shall test multiple approaches to injecting reagents into the reactor chamber to optimize mixing and uniform distribution of reagent gases. THE RECIPIENT shall optimize growth parameters such as temperature, pressure, V:III ratio, carrier flow rate, and total gas flow. u-GaN and MQW layer thickness uniformities shall be monitored both within wafer (w-i-w) and wafer to wafer (w-2-w) across a multi-wafer carrier. The recipient shall have the goal of controlling GaN layer thickness uniformity with a standard deviation below 2%. THE RECIPIENT shall optimize the chamber design for the requisite temperature control. The HVPE system shall have a goal of achieving contaminant levels below 10^{16} atoms/cm3 for chlorine and oxygen. The HVPE system shall be suitable for a cluster deposition system that also incorporates MOCVD chambers. At the end of Task 2, THE RECIPIENT shall test the system for the following criteria:

- Growth of 4-micron GaN layer
- Temperature uniformity across the carrier
- GaN thickness uniformity within the wafer
- GaN thickness uniformity wafer-to-wafer
- GaN crystalline quality (threading dislocations per cm^2)
- Contaminant levels for Oxygen and Chlorine

Epi Tool with multi Chamber Split Process

THE RECIPIENT shall design and build a multi-chamber, split-process Epi tool that with the goal of increasing throughput and minimizing PL wavelength drift. The system shall have the ability to grow HT-GaN template in one chamber and MQW layers in another chamber. THE RECIPIENT shall have a target both w-i-w and w-2-w PL wavelength uniformity of 2 nm or better. THE RECIPIENT shall integrate precise multi-zone temperature controls and process gas flow controls into the production ready Epi tool. THE RECIPIENT shall develop a process recipe with the goal of optimizing the multi-chamber system such as a MOCVD / HVPE (2+1) system described above to be capable of fabricating LEDs with internal quantum efficiency up to 75%. THE RECIPIENT shall test the multi-chamber MOCVD / HVPE system for the following properties:

- EL Uniformity Within the Wafer
- PL Uniformity Within the Wafer
- PL Uniformity Wafer-to-Wafer
- PL Uniformity Run-to-Run
- Run-to-Run Std. Dev.
- IQE

Process for Growing Low-Defect, High-Quality LED Structures on the Most Industrially Relevant Substrates

THE RECIPIENT shall have the goal of demonstrating that the multi-chamber, split-process Epi prototype developed in Task 3 can deposit high-quality GaN material (including ternary and quaternary alloys) on at least two substrates. The process development shall focus on optimizing crystal quality and uniformity, and exploring process parameters with a goal of elucidating GaN, GaInN, and AlInGaN epitaxial growth mechanisms.

In-Situ Cleaning Process

THE RECIPIENT shall develop an *in situ* cleaning process for the MOCVD chamber using halogen-based etching gases, with the goal of delivering a clean showerhead, with minimal residual $GaCl_3$, that does not adversely affect the crystal quality of the GaN layers in a subsequent run. THE RECIPIENT shall demonstrate *in situ* cleaning time with a goal of reaching 1 hour clean time. THE RECIPIENT shall have a goal that the *in situ* cleaning makes it possible to complete at least 5 MOCVD chamber runs without breaking vacuum and without affecting the crystal quality of LED structures created in the next run or in succeeding runs.

Optimized multi-Chamber Epi Tool

THE RECIPIENT shall assemble an optimized multi-chamber system such as a MOCVD / HVPE (2+1) system capable of growing high quality HB-LEDs with low defect densities on multi-wafer carriers. THE RECIPIENT shall equip the MOCVD process chambers with *in situ* cleaning capability for enhanced throughput, high binning yield, and minimal deviations in PL/EL/thickness uniformity.

Approaches used

Key aspects to our technical approach are itemized below.

1. Validate our baseline approach for low-cost split process GaN growth: focus on each layer and then on integration
    a. u-GaN/n-GaN (Si-doped)
    b. MQW
    c. p-GaN (Mg-doped)
2. Create a multi-chamber MOCVD / HVPE system (2 MOCVD +1 HVPE).
3. Create a novel subsystem for automated *in situ* cleaning of the deposition chambers.
4. Control the growth temperature with precision high-speed lamp heating.
5. Reduce material defects by taking advantage of the flexible configuration of Applied Material's Centura™ deposition chambers.

The multi-chamber architecture enabled an innovative approach to growing the hetero-epitaxial layer by using dedicated chambers for each of the major segments in the epi stack: u-GaN/n-GaN, MQW, and p-GaN.

Problems encountered

HVPE uniformity from wafer to wafer was a challenge that we overcame, but took longer than expected to validate. The challenges and progress in our HVPE development was reported monthly to our program manager.

The main unforeseen issue for this program, however, was the market condition for LED GaN epi tools after early 2011. The so-called “crash” in tool sales for the LED industry was unexpected in its severity and suddenness. Additionally, since Applied was new to the market, customers demanded that we demonstrate world class LEDs and process controls before purchasing agreements could be completed. This caused understandable delays and although we were able to demonstrate world-class results as described above, the market collapse limited the sales in 2012.

The future of the tool developed, however, is especially bright for GaN on silicon manufacturing given the ability to separate processes as well as cost-effective large diameter (>12”) thick GaN templates with GaN thickness greater than 20um.

Products developed under the award

Networks or collaborations fostered

Strong partnerships were fostered with academia, national labs, and other companies through this program. We found the DOESSL Workshops very helpful in making contacts and fostering discussions. One particularly strong collaboration was with Sandia National Labs for third party validation of our GaN process and metrology we were not able to perform, which was particularly helpful to Applied Materials.

Technologies/Techniques

A number of key technologies as shown by the inventions below were developed during the course of this program which helped Applied Materials develop key technologies for the GaN epi market. In addition, jobs were created and saved in Santa Clara, California

Inventions/Patent Applications

Five patent applications were submitted through this program thanks to the support of the DOE:

Summary

Over the course of this program, Applied Materials, Inc., with generous support from the United States Department of Energy, developed a world-class three chamber III-Nitride epi cluster tool for low-cost, high volume GaN growth for the solid state lighting industry. One of the major achievements of the program was to design, build, and demonstrate the world's largest wafer capacity HVPE chamber suitable for repeatable high volume III-Nitride template and device manufacturing.

Applied Materials' experience in developing deposition chambers for the silicon chip industry over many decades resulted in many orders of magnitude reductions in the price of transistors. That experience and understanding was used in developing this GaN epi deposition tool. The multi-chamber approach, which continues to be unique in the ability of the each chamber to deposit a section of the full device structure, unlike other cluster tools, allows for extreme flexibility in the manufacturing process. This robust architecture is suitable for not just the LED industry, but GaN power devices as well, both horizontal and vertical designs.

The new HVPE technology developed allows GaN to be grown at a rate unheard of with MOCVD, up to 20x the typical MOCVD rates of 3μm per hour, with bulk crystal quality as better than the highest-quality commercial GaN films grown by MOCVD at a much cheaper overall cost. This is a unique development as the HVPE process has been known for decades, but never successfully commercially developed for high volume manufacturing. This research shows the potential of the first commercial-grade HVPE chamber, an elusive goal for III-V researchers and those wanting to capitalize on the promise of HVPE.

Additionally, in the course of this program, Applied Materials built two MOCVD chambers, in addition to the HVPE chamber, and a robot that moves wafers between them. The MOCVD chambers demonstrated industry-leading wavelength yield for GaN based LED wafers and industry-leading uptime enabled in part by a novel in-situ cleaning process developed in this program.

The Department of Energy was a great supporter of this leading-edge technology that can benefit U.S. industry and keep GaN manufacturing competitive in the United States. We gratefully acknowledge their role in advancing the state-of-the-art.

Acknowledgements

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We gratefully acknowledge the hard work of the DOE in developing and managing this important program. We particularly are grateful to or program manager, Brian Dotson of NETL, who has guided us and provided very helpful advice.

Also, we wish to thank Jim Brodrick, the solid-state lighting (SSL) portfolio manager in the DOE's Office of Energy Efficiency and Renewable Energy. His vision for solid state lighting and manufacturing helped to successfully execute programs like ours which are key in providing the investment in driving technology forward.

Finally, we wish to thank Sean Evans, our initial program manager at NETL.